

S/N-09/551,027

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al.

Serial No.: 09/551,027

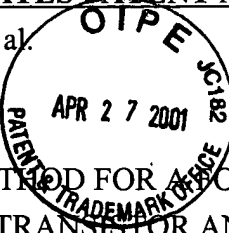
Filed: April 17, 2000

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

Examiner: Michael Trinh

Group Art Unit: 2822

Docket: 303.379US2



PATENT

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AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

This amendment and response is being resubmitted with corrections to the specification per the Notice of Non-compliant Amendment mailed on March 30, 2001. The fee for additional claims was paid in the previously filed amendment and response on March 21, 2001.

Applicant has carefully reviewed the Office Action mailed December 21, 2000. Detailed comments to the Office Action are found in the Remarks section below. Amendments to the specification and claims are found in the following Amendments section.

IN THE SPECIFICATION

Please substitute the following paragraph that begins on Page 9, line 26 and ends on Page 10, line 3 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into [first] second source/drain region 206, body region 208, and [second] first source/drain region 210 to form access transistor 211. Pillar 204 extends vertically outward from substrate 212 of, for example, p- silicon. [First] Second source/drain region 206 and [second] first source/drain region 210 each comprise, for example, n + silicon and body region 208 comprises p- silicon.



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DATE: 10/17 PAGE: 17/100 NOBLE

EXAMINER

ART UNIT

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Legal Instruments Examiner

Schweyhan, Lundberg
Woessner & Kluth P.A.

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